Remarks

The present amendment responds to the Official Action dated March 30, 2004. The Official Action rejected claims 1, 44-52, and 57-59 under 35 U.S.C. 102(a) based on Figs. 1 and 2 labeled "prior art" in the specification. Claims 1, 44-52 and 57-59 were also rejected under 35 U.S.C. 102(b) based on Barker et al. U.S. Patent No. 5,717,943 (Barker). These grounds for rejection are addressed below.

Claims 2-43 and 53-56 have been previously cancelled without prejudice. Claims 1 and 44 have been amended to be more clear and distinct. Specifically, claims 1 and 44 have been amended to clarify that the arrangement of PEs into clusters are based on each PE corresponding to an element in a matrix of PEs. Further, claims 1 and 44 have been amended to show how the connections between PEs are reduced. Claims 1, 44-52 and 57-59 are presently pending.

The Art Rejections

All of the art rejections hinge on the application of Figs. 1 and 2 of the present specification or upon Barker. As addressed in greater detail below, Figs. 1 and 2 of the specification and Barker do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicant does not acquiesce in the analysis of Barker made by the Official Action and, in light of the present amendment, respectfully traverses the Official Action's analysis underlying its rejections.

The Official Action rejected claims 1, 44-52, and 57-59 under 35 U.S.C. 102(a) based on Figs. 1 and 2 labeled "prior art" in the specification. Figs. 1 and 2 demonstrate the connections

between processing elements in a prior art 4x4 torus arrangement. Turning to page 2, line 30 et seq. of the *Background of the Invention* section, Fig. 1A illustrates wraparound connections between sixteen processing elements connected in a four by four array of PEs. Based on the number of PEs, 32 wires are necessary for interconnecting between all the PEs. For an NxN array of N^2 PEs similarly connected, the number of wire connections is $2kN^2$ where $k = 1$ for a bidirectional wire. Turning to page 7, lines 23-26, Figs. 1B and 1C illustrate alternative physical wire connections between two processing elements for the torus connection paths of Fig. 1A. Fig. 1B illustrates T transmit and R receive unidirectional wires. Fig. 1C illustrates B bidirectional wires. Turning to Fig. 2, a prior art approach is illustrated which positions PEs to be in close proximity with their transpose PEs by folding the array of PEs. At page 5, lines 18-21 of the specification, it is indicated that while folding the array reduces inter-PE wiring, it continues to require physical wires between PEs which limit the operation of PEs to operate as defined by a fixed topology. It should be noted that a distinction is not made between the logical arrangement of elements in a matrix and the physical arrangement of PEs in Figs. 1. With regard to Fig. 2, the only distinction made between the logical arrangement and the physical arrangement is that the logical matrix of PE elements is transformed by folding the logical matrix at its diagonal to create the physical arrangement.

In contrast, the present invention addresses an interconnection system which reduces the number of physical wires between processing elements while preserving the interconnectivity paths between the processing elements. To this end, the present invention introduces a cluster arrangement of PEs where the assignment of PEs to each cluster depends on each PE's logical

position in a matrix. For example, a PE may be logically viewed by a programmer as an element of a matrix. From such a perspective, each PE performs operations associated with a particular element positioned in a matrix. However, due to the wiring limitations resulting from laying out the PEs in a semiconductor chip, the present invention separates this logical view from a physical view. In so doing, the physical view which represents how the PEs are layed out in one or more semiconductor chips includes arranging the PEs into clusters. Since a PE, in the present invention, corresponds to a position in a matrix, the determination of which PEs populate a cluster depends on the neighbors relative to the matrix position of each PE. From a logical view, a PE based on its position in the matrix has matrix position neighbors to its North, East, South and West. Due to the fact that in typical operation all PEs communicate in the same direction, a pair of neighbors are said to be mutually exclusive when one neighbor is to the North or South of the PE's position and the other neighbor is to the East or West of the PE's position.

Referring to Fig. 5, for example, assuming $PE_{2,0}$ were assigned to cluster 1 labeled 48, it's neighbor to the North, $PE_{1,0,}$ would be assigned to another cluster, cluster 2 labeled 46, and it's neighbor to the East, $PE_{2,1}$, would be assigned to yet another cluster, cluster 3 labeled 50. In general, the clusters are populated by determining the mutually exclusive matrix position neighbors of each PE and assigning each pair of mutually exclusive neighbors to at most two clusters. Referring to Fig. 16, for example, these PEs would be physically layed out in one or more semiconductor chips as illustrated. Cluster 48 would communicate through cluster switch 86 to cluster 50. It should be noted that transmit lines 88 illustrate a sharing of transmit lines between PEs that share matrix position neighbors resulting in a reduction of transmit lines for

connectivity. For example, $PE_{2,1}$ is a matrix position neighbor to both $PE_{2,3}$ and $PE_{3,3}$. Consequently, only one transmit line terminates at $PE_{2,1}$ and is shared by $PE_{2,3}$ and $PE_{3,3}$. This arrangement of PEs advantageously requires fewer wires to achieve a desired connectivity between PEs. Further, this arrangement promotes componentizing each cluster on its own semiconductor chip and limiting the connections between separate semiconductor chips.

Claim 1, as presently amended, reads as follows:

> 1. An interconnection system for a plurality of processing elements (PEs), each PE having a communications port for transmitting and receiving data and commands, each PE corresponding to a position of a matrix element where the position of the matrix element has at least a North, East, South, or West matrix position neighbor, a pair of matrix neighbors is mutually exclusive when one neighbor is either in the North or South direction relative to the position of the matrix element and the other neighbor is either in the East or West direction relative to the position, the interconnection system comprising:
>
> a plurality of clusters of PEs, each cluster comprising a portion of the plurality of PEs; and
>
> a cluster switch connected to said PEs in each cluster, said portion of the plurality of PEs assigned so that each PE in said portion of the plurality of PEs has its mutually exclusive matrix position neighbors in at most two of the plurality of clusters of PEs, at least two PEs in one cluster sharing a connection to their common neighbor in another cluster when communicating to their mutually exclusive matrix position neighbors through the cluster switch. (emphasis added)

Figs. 1 and 2 address a conventionally connected torus array which provides either no transformation or a limited folding transformation between a logical view and its corresponding physical view. Figs. 1 and 2 do not disclose and do not make obvious assigning PEs to a plurality of clusters as claimed. Further Figs. 1 and 2 do not disclose and do not make obvious assigning PEs to a plurality of clusters in the manner as presently claimed. See also claim 44 which has been similarly amended.

The Official Action also rejected claims 1, 44-52, and 57-59 under 35 U.S.C. 102(a) based on Barker. Barker describes an array architecture which is termed "brick technology" because a basic building brick consisting of a network node 310 shown in Fig. 6 is employed. A basic sub-component within the network node is the processor memory element (PME). The eight PMEs within the network node 310 are interconnected in a pattern resulting in the three dimensional cube structure shown in Barker's Fig.10. Barker, col. 40, lines 44-45. Each PME is interconnected with its three neighbors using a set of input/output ports providing full duplex communication capability between PMEs, as further illustrated in Figs. 10 and 11, and described at Barker, col. 39, lines 48-51. Referring to col. 40, lines 48-49, an nxn array of nodes is a cluster. An array of clusters results in a 4 dimensional torus or hypercube structure. Barker, col. 40, lines 61-62. Barker does not disclose how PEs are assigned to individual clusters and, thus, does not disclose arranging PEs into clusters in the manner as presently claimed.

In stark contrast, the present invention assigns PEs to clusters by determining the mutually exclusive matrix position neighbors of each PE and assigning each pair of mutually exclusive neighbors to at most two clusters. Claim 1, as presently amended, recites "each cluster comprising a portion of the plurality of PEs" and "said portion of the plurality of PEs assigned so that each PE in said portion of the plurality of PEs has its mutually exclusive matrix position neighbors in at most two of the plurality of clusters." Claim 44, as presently amended, recites "the plurality of PEs arranged in a plurality of clusters, each cluster including a portion of the plurality of processing elements, the portion of the plurality of PEs selected so that each PE in said portion of the plurality of PEs has its mutually exclusive matrix position neighbors in at

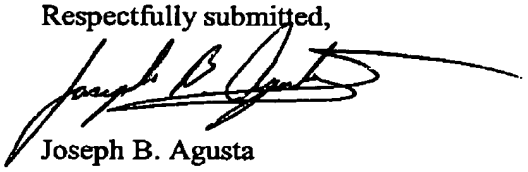
most two of the plurality of clusters." Further, the present invention reduces connections between clusters by sharing a wire between a PE and a second PE in the same cluster when communicating to a common neighbor PE located in another cluster. Claim 1, as presently amended, recites "at least two PEs in one cluster sharing a connection to their common neighbor in another cluster when communicating to their mutually exclusive matrix position neighbors through the cluster switch." Claim 44, as presently amended, recites "at least two PEs in each cluster share a connection to their common neighbor to another cluster through the cluster switch."

Barker does not disclose and does not claim arranging PEs in a cluster in the manner presently claimed. Barker does not disclose and does not claim "at least two PEs in one cluster share a connection to their common neighbor in another cluster when communicating to their mutually exclusive matrix position neighbors through the cluster switch" as presently claimed in claim 1. Barker does not disclose and does not claim "at least two PEs in each cluster sharing a connection to their common neighbor to another cluster through the cluster switch" as presently claimed in claim 44.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



Joseph B. Agusta
Reg. No. 52,547
Priest & Goldstein, PLLC
5015 Southpark Drive, Suite 230
Durham, NC 27713-7736
(919) 806-1600